FIG. 1

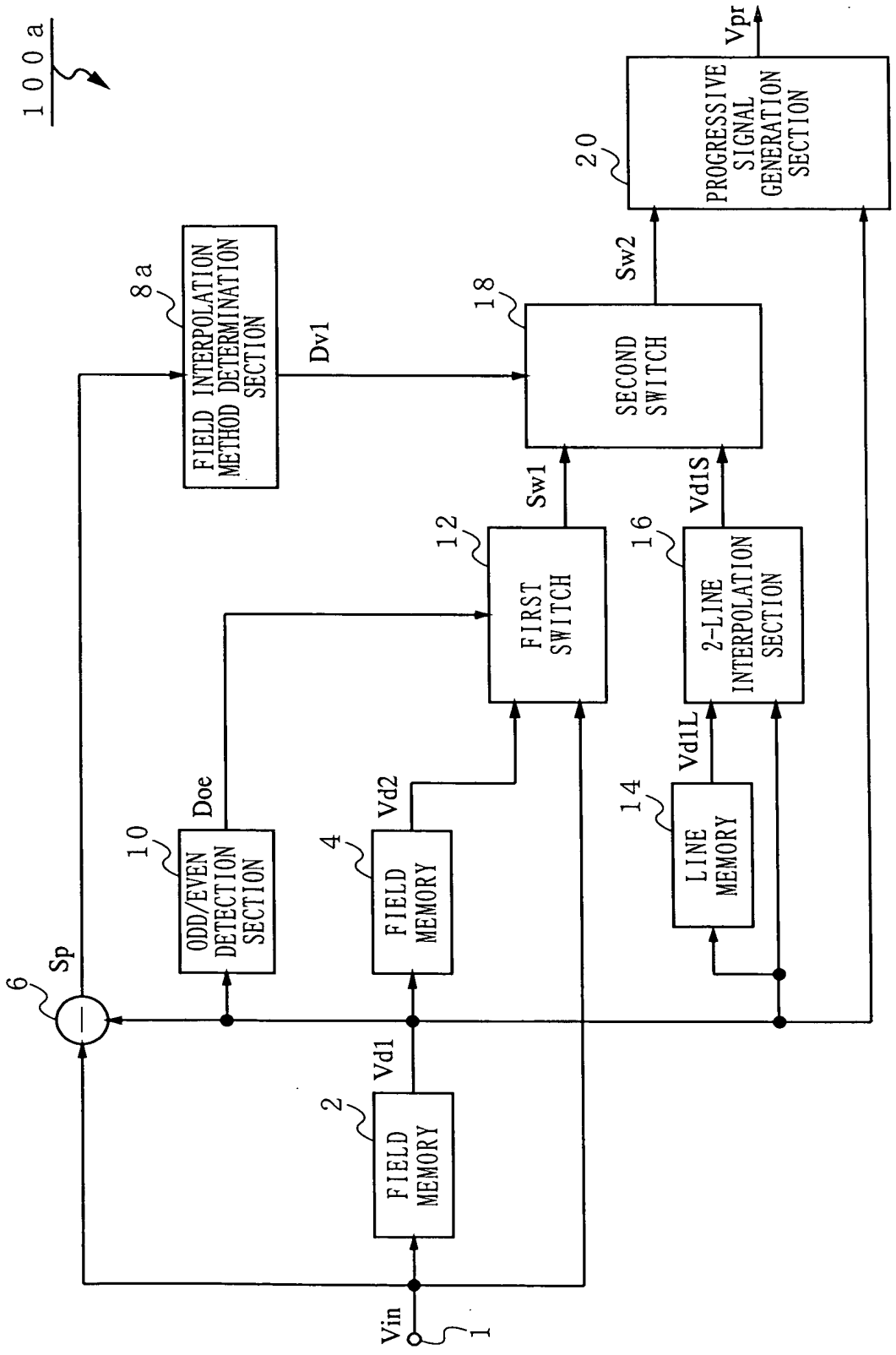

100a
Vin
1
FIELD MEMORY
2
Vd1
FIELD MEMORY
4
Vd2
ODD/EVEN DETECTION SECTION
10
Doe
Sp
6
FIELD INTERPOLATION METHOD DETERMINATION SECTION
8a
Dv1
FIRST SWITCH
12
Sw1
LINE MEMORY
14
Vd1L
2-LINE INTERPOLATION SECTION
16
Vd1S
SECOND SWITCH
18
Sw2
PROGRESSIVE SIGNAL GENERATION SECTION
20
Vpr

FIG. 2

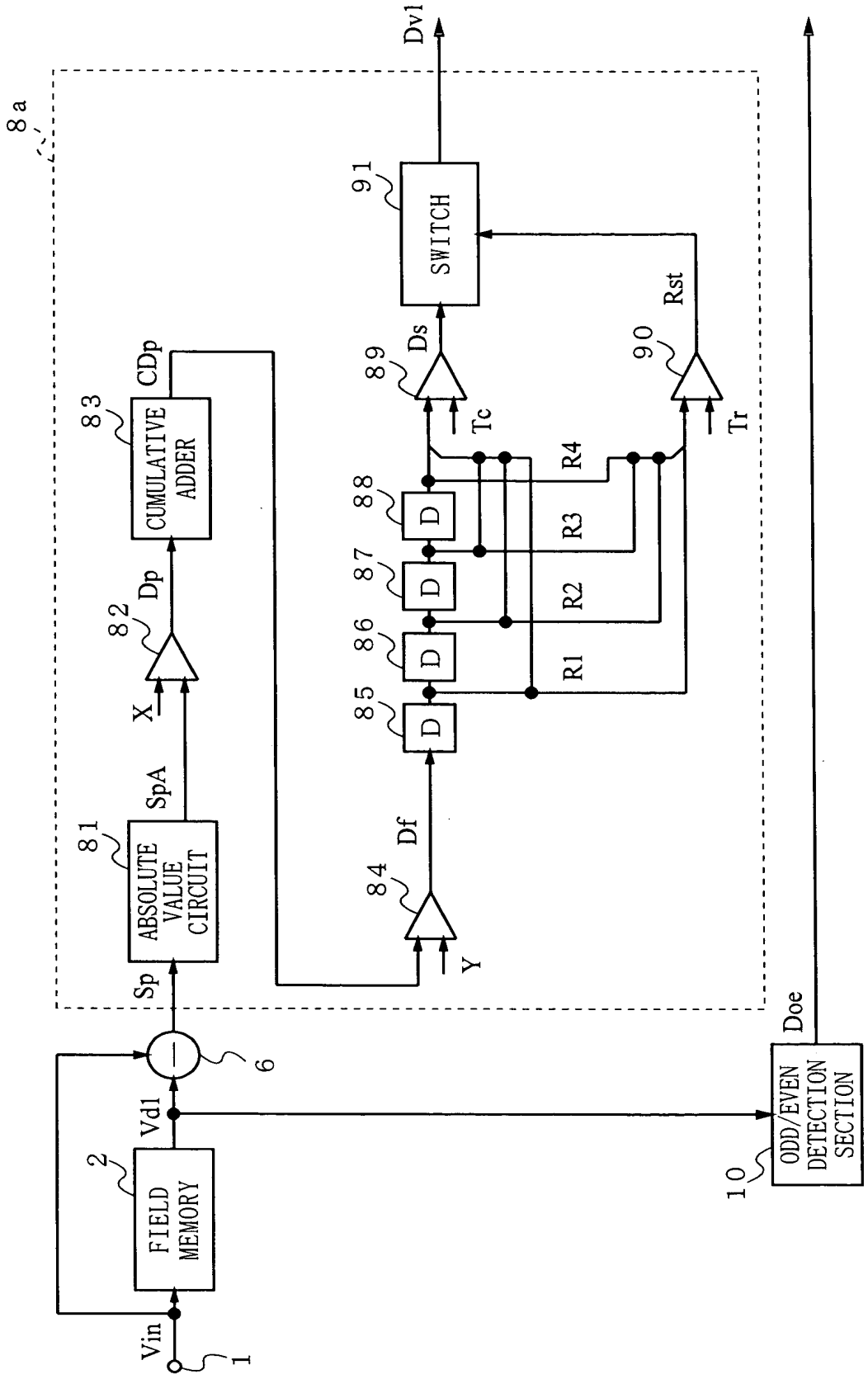

Vin
1
FIELD MEMORY
2
Vd1
6
Sp
8a
ABSOLUTE VALUE CIRCUIT
81
SpA
X
82
Dp
CUMULATIVE ADDER
83
CDp
Df
84
Y
D
85
D
86
D
87
D
88
R1
R2
R3
R4
Ds
89
Tc
Rst
90
Tr
SWITCH
91
Dv1
Doe
ODD/EVEN DETECTION SECTION
10

FIG. 3

| REGISTER 85 R1 | REGISTER 86 R2 | REGISTER 87 R3 | REGISTER 88 R4 | COUNTER INPUT | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | INCREMENT | Tc |
| 1 | 0 | 1 | 0 | INCREMENT | |
| 0 | 0 | 0 | 0 | CANCEL | T1 |
| 0 | 0 | 0 | 1 | CANCEL | |
| 0 | 0 | 1 | 0 | CANCEL | |
| 0 | 1 | 0 | 0 | CANCEL | |
| 1 | 0 | 0 | 0 | CANCEL | |
| 0 | 0 | 1 | 1 | RESET | Tr |
| 0 | 1 | 1 | 0 | RESET | |
| 0 | 1 | 1 | 1 | RESET | |
| 1 | 0 | 0 | 1 | RESET | |
| 1 | 0 | 1 | 1 | RESET | |
| 1 | 1 | 0 | 0 | RESET | |
| 1 | 1 | 0 | 1 | RESET | |
| 1 | 1 | 1 | 0 | RESET | |
| 1 | 1 | 1 | 1 | RESET | |

FIG. 4

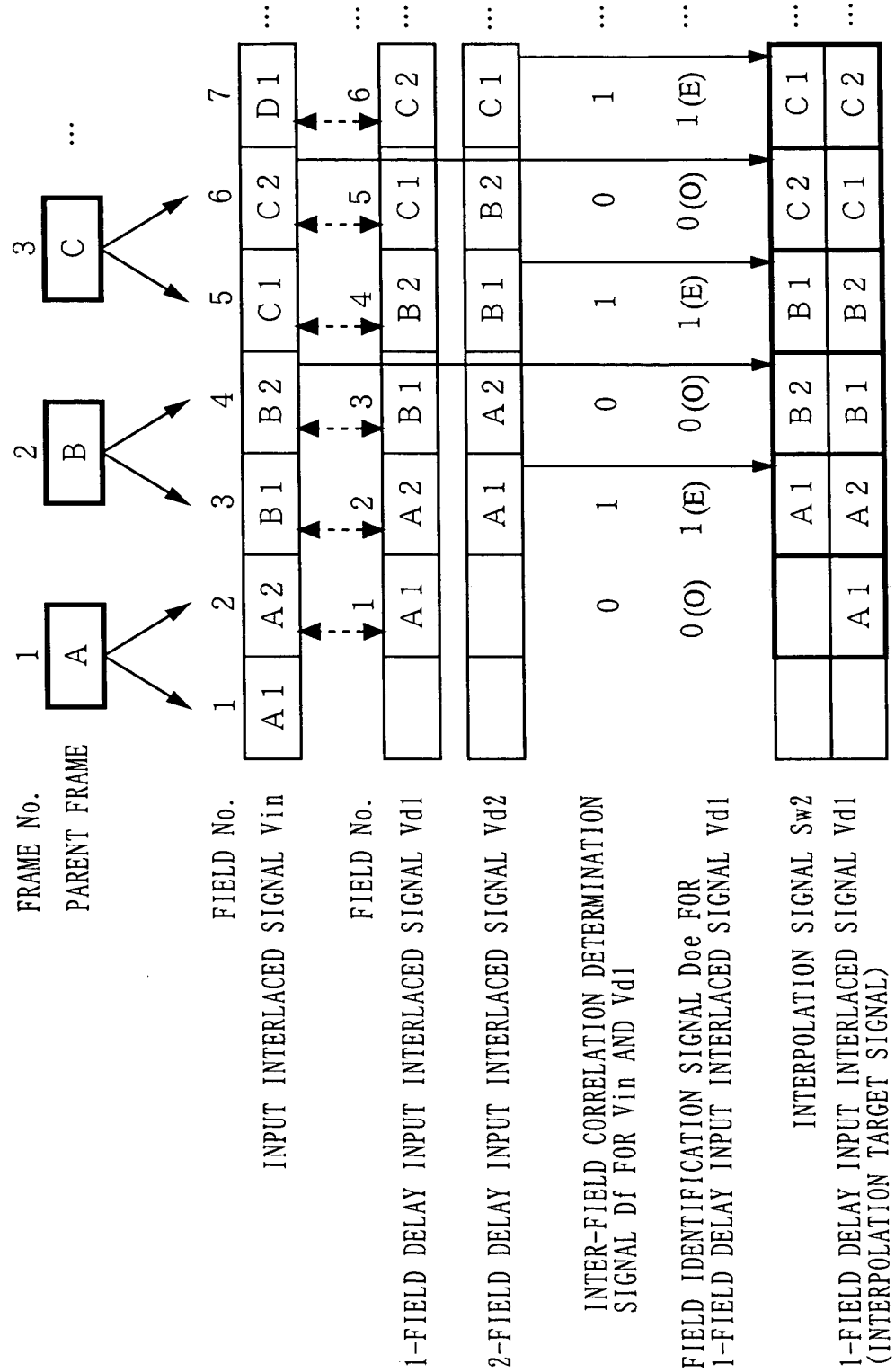

FRAME No.
PARENT FRAME
1
A
2
B
3
C
...
FIELD No.
INPUT INTERLACED SIGNAL Vin
1-FIELD DELAY INPUT INTERLACED SIGNAL Vd1
2-FIELD DELAY INPUT INTERLACED SIGNAL Vd2
INTER-FIELD CORRELATION DETERMINATION SIGNAL Df FOR Vin AND Vd1
FIELD IDENTIFICATION SIGNAL Doe FOR 1-FIELD DELAY INPUT INTERLACED SIGNAL Vd1
INTERPOLATION SIGNAL Sw2
1-FIELD DELAY INPUT INTERLACED SIGNAL Vd1 (INTERPOLATION TARGET SIGNAL)
A1
A2
B1
B2
C1
C2
D1
0
1
0(O)
1(E)

FIG. 5

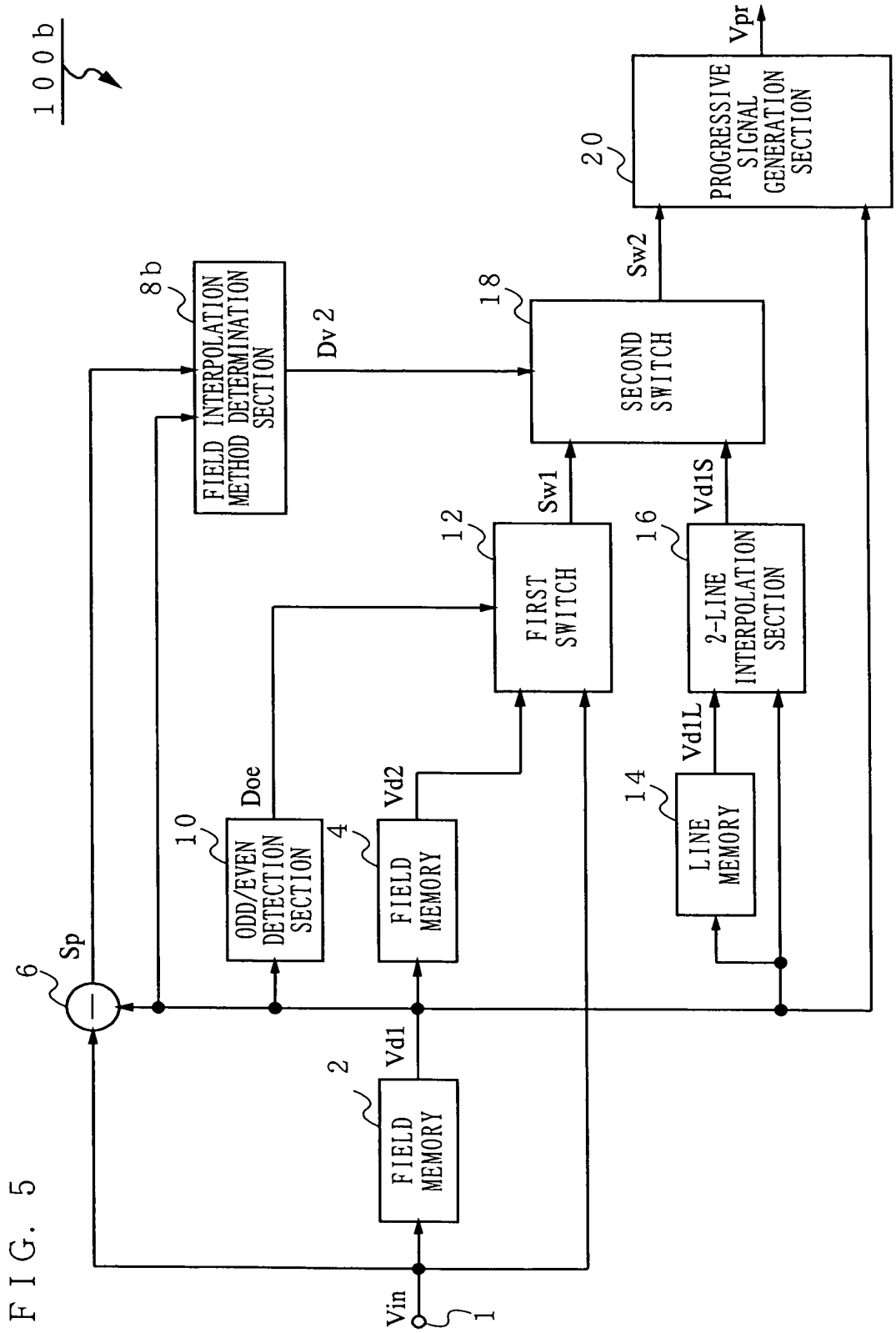

100b
Vpr
20
PROGRESSIVE SIGNAL GENERATION SECTION
Sw2
18
SECOND SWITCH
8b
FIELD INTERPOLATION METHOD DETERMINATION SECTION
Dv2
Sw1
12
FIRST SWITCH
Vd1S
16
2-LINE INTERPOLATION SECTION
Doe
10
ODD/EVEN DETECTION SECTION
Vd2
4
FIELD MEMORY
Vd1L
14
LINE MEMORY
Sp
6
Vd1
2
FIELD MEMORY
Vin
1

FIG. 6

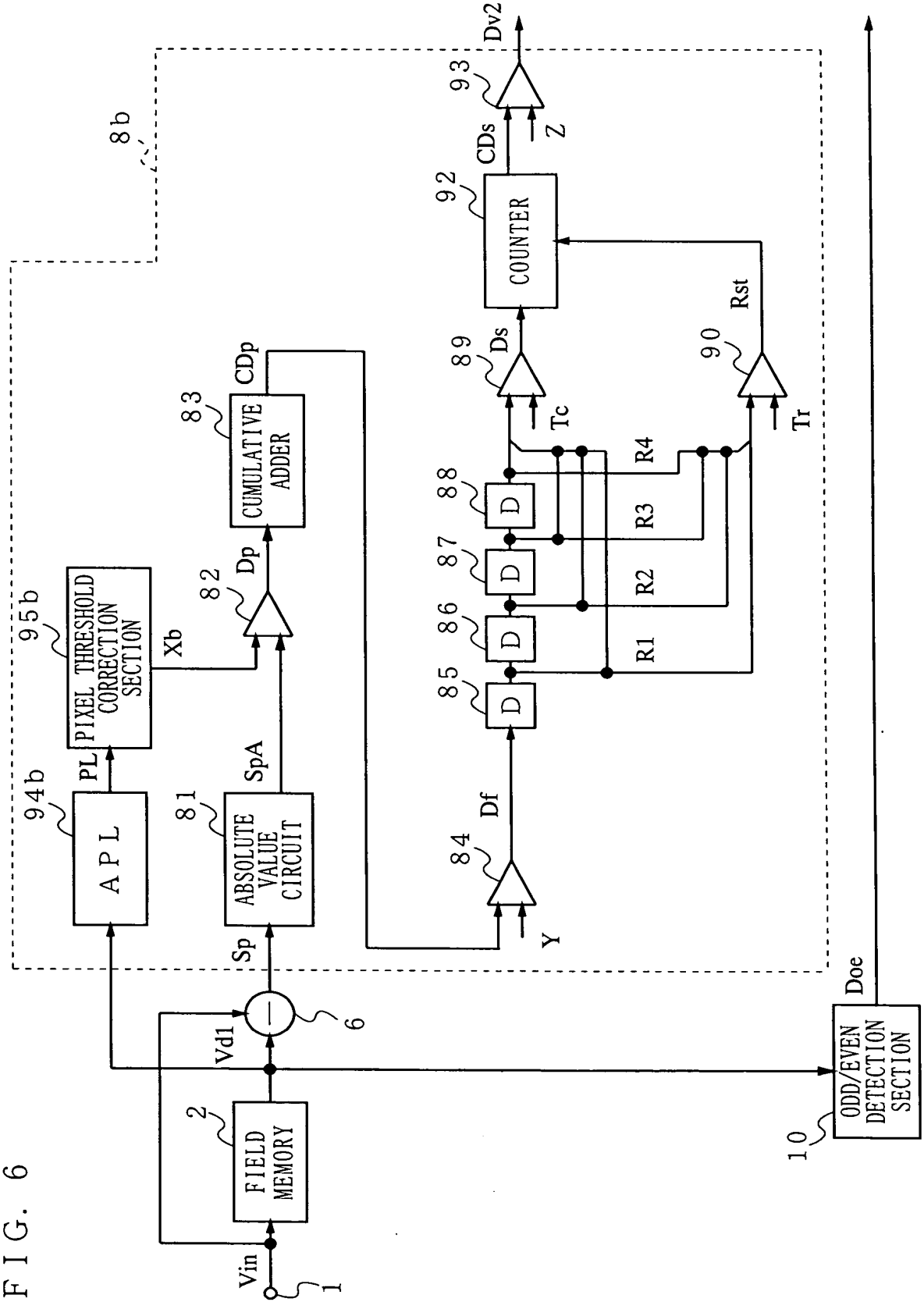

8b
Vin
1
FIELD MEMORY
2
Vd1
6
Sp
APL
94b
PL
PIXEL THRESHOLD CORRECTION SECTION
95b
Xb
ABSOLUTE VALUE CIRCUIT
81
SpA
CUMULATIVE ADDER
83
CDp
Dp
82
Df
84
D
85
D
86
D
87
D
88
R1
R2
R3
R4
Tc
89
Ds
Tr
90
Rst
COUNTER
92
CDs
93
Dv2
Z
Y
Doe
ODD/EVEN DETECTION SECTION
10

FIG. 7

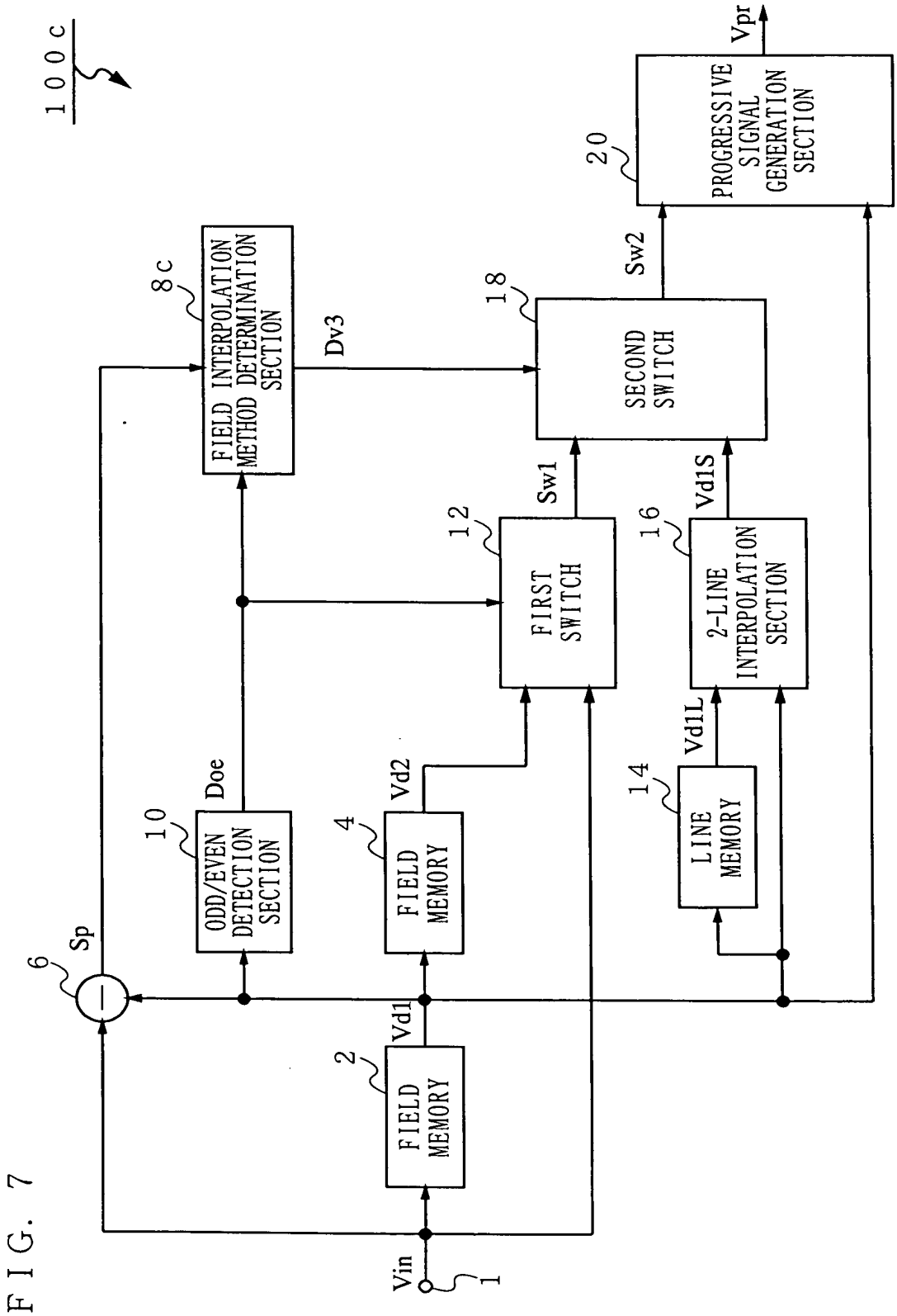

100c
Vpr
20
PROGRESSIVE SIGNAL GENERATION SECTION
Sw2
18
SECOND SWITCH
8c
FIELD INTERPOLATION METHOD DETERMINATION SECTION
Dv3
Sw1
12
FIRST SWITCH
Vd1S
16
2-LINE INTERPOLATION SECTION
Vd1L
14
LINE MEMORY
Doe
10
ODD/EVEN DETECTION SECTION
Vd2
4
FIELD MEMORY
Sp
6
Vd1
2
FIELD MEMORY
Vin
1

FIG. 8

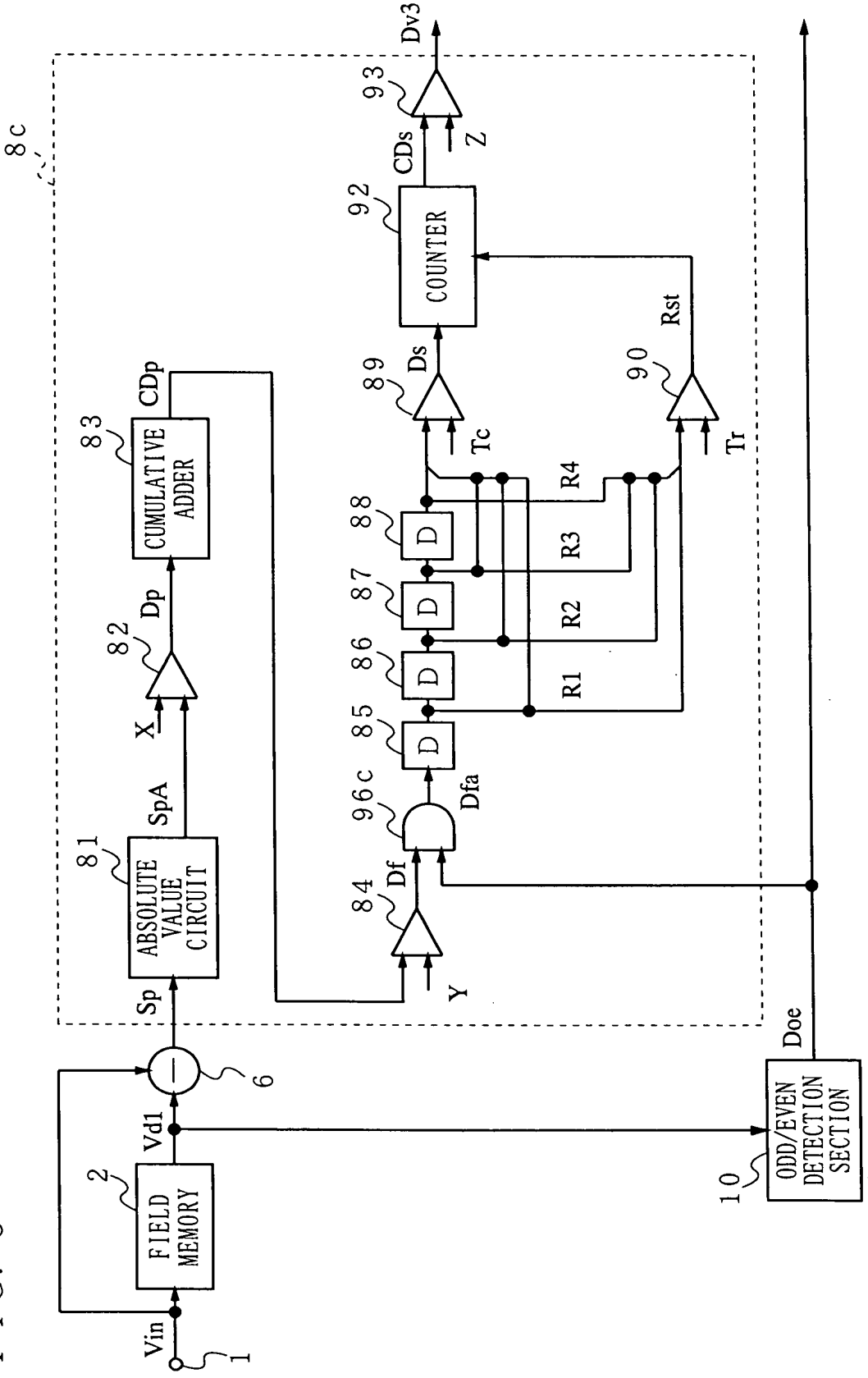

8c
Vin
1
FIELD MEMORY
2
Vd1
6
Sp
ABSOLUTE VALUE CIRCUIT
81
SpA
X
82
Dp
CUMULATIVE ADDER
83
CDp
Df
84
Y
96c
Dfa
D
85
D
86
D
87
D
88
R1
R2
R3
R4
Ds
89
Tc
Rst
90
Tr
COUNTER
92
CDs
Z
93
Dv3
Doe
ODD/EVEN DETECTION SECTION
10

FIG. 9

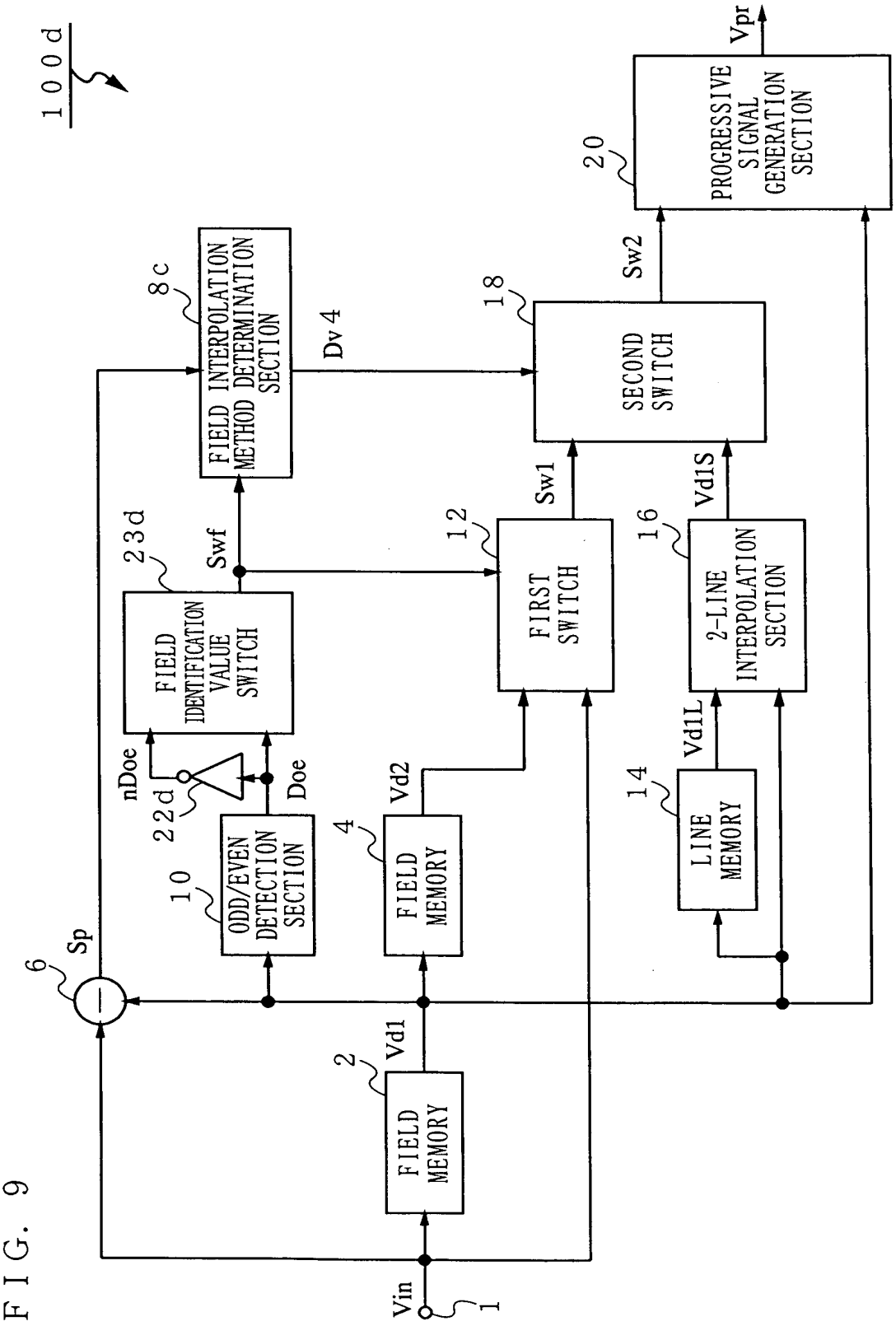

100d
Vin
1
FIELD MEMORY
2
Vd1
FIELD MEMORY
4
Vd2
LINE MEMORY
14
Vd1L
ODD/EVEN DETECTION SECTION
10
nDoe
22d
Doe
FIELD IDENTIFICATION VALUE SWITCH
23d
Swf
FIELD INTERPOLATION METHOD DETERMINATION SECTION
8c
Dv4
6
Sp
FIRST SWITCH
12
Sw1
2-LINE INTERPOLATION SECTION
16
Vd1S
SECOND SWITCH
18
Sw2
PROGRESSIVE SIGNAL GENERATION SECTION
20
Vpr

FIG. 10

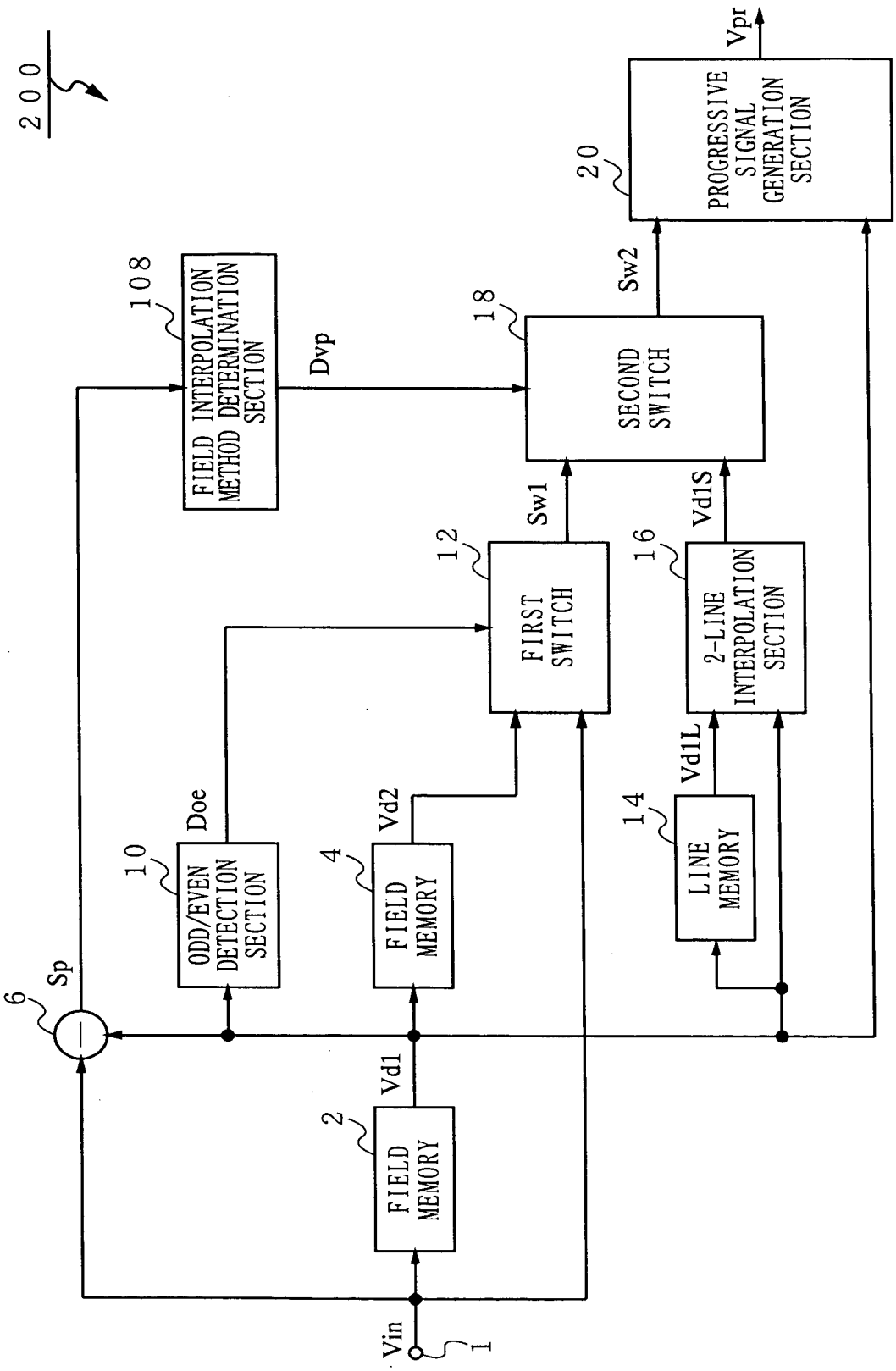
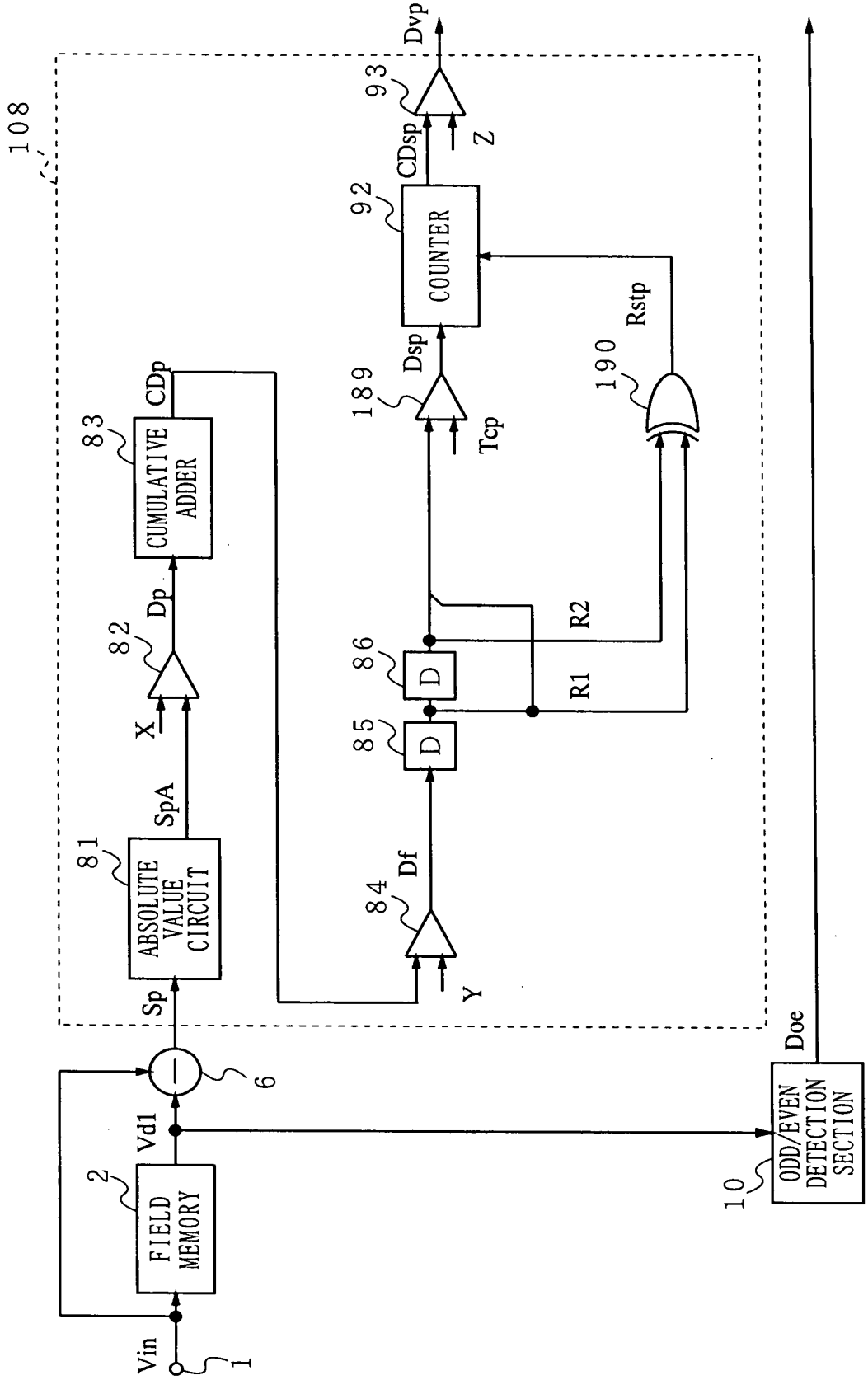

200
Vpr
PROGRESSIVE SIGNAL GENERATION SECTION
20
Sw2
SECOND SWITCH
18
Dvp
FIELD INTERPOLATION METHOD DETERMINATION SECTION
108
Sw1
Vd1S
FIRST SWITCH
12
2-LINE INTERPOLATION SECTION
16
Doe
Vd2
Vd1L
ODD/EVEN DETECTION SECTION
10
FIELD MEMORY
4
LINE MEMORY
14
Sp
6
Vd1
FIELD MEMORY
2
Vin
1

FIG. 11


Vin
1
FIELD MEMORY
2
Vd1
6
Sp
ABSOLUTE VALUE CIRCUIT
81
SpA
X
82
Dp
CUMULATIVE ADDER
83
CDp
Df
84
Y
D
85
D
86
R1
R2
Dsp
189
Tcp
COUNTER
92
CDsp
Z
93
Dvp
Rstp
190
108
Doe
ODD/EVEN DETECTION SECTION
10